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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,460	03/22/2004	Koji Sakui	250849US2S	9023

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EXAMINER	
HOANG, HUAN	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,460	SAKUI, KOJI	
	Examiner	Art Unit	
	Huan Hoang	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,20-35 and 38-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-17,20-25,27-35 and 38-40* is/are rejected.

7)☐ Claim(s) *7,8 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *032204 & 062005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 18,19, 36, 37 and 41-87 have been canceled by Applicant.

2. Applicant's election of Group I in the reply filed on 10/11/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Objections

3. Claims 12 and 30 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 11 and 29, respectively. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

All the limitations of claims 12 and 30 are recited in claims 11 and 29, respectively.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 9, 10, 13, 14, 20-23, 27, 28, 31 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al..

Lee et al. discloses a nonvolatile semiconductor memory having all the elements as recited in claims 1-4, 9, 10, 13, 14, 20-23, 27, 28, 31 and 32 as follows:

first cells units (Fit. 16) each comprising one memory cell and tow select gate transistors;

a word line (WL00, Fig. 16) connected in common to each cell of the first cell units;

bit lines (BL0(0) ... BL7(0), Fig. 16) individually connected to the first cell units;

sense amplifiers disposed for the bit lines (Fig. 27 and column 29, lines 39-40), an erase circuit which divides the first cell units in to blocks and which sets potentials of the bit lines (Table 1 and Table 2, column 13 and column 14) by a block unit at an erase time (Abstract, line 3 and column 3, lines 35-42);

wherein each of the blocks includes the first cell units for one byte (Abstract);

wherein at the erase time, data is erased by the block unit (byte erase, Abstract);

wherein wells are disposed for the blocks, and the first cell units are disposed in the same well by the block unit (Fig. 14);

wherein at the erase time, the data erase comprises generating a high electric field between a drain and a control gate electrode of the memory cell which is an erase object; and extracting electrons into the drain region from a floating gate electrode (column 25, lines 26-33).

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-6, 9, 10, 13-17, 20-25, 27, 28, 31-35 and 38-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakui et al. (US Patent No. 6,307,807 cited by Applicant).

Sakui et al. discloses a nonvolatile semiconductor memory having all the elements as recited in claims 1-6, 9, 10, 13-17, 20-25, 27, 28, 31-35 and 38-40 as follows:

first cells units (Fig. 26) each comprising one memory cell and tow select gate transistors;

a word line (CGL, Fig. 26) connected in common to each cell of the first cell units;

bit lines (BL0 ... BL511, Fig. 26) individually connected to the first cell units;

sense amplifiers disposed for the bit lines (Fig. 26) an erase circuit which divides the first cell units in to blocks and which sets potentials of the bit lines (Table 1 to Table 4) by a block unit at an erase time;

wherein each of the blocks includes the first cell units for one byte;

wherein at the erase time, data is erased by the block unit ;

wherein wells are disposed for the blocks, and the first cell units are disposed in the same well by the block unit;

wherein at the erase time, the data erase comprises generating a high electric field between a drain and a control gate electrode of the memory cell which is an erase object; and extracting electrons into the drain region from a floating gate electrode.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 11, 12, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al or Sakui et al. in view of Hemink et al..

Lee et al. or Sakui et al. discloses all the limitations of claims 11, 12, 29 and 30 except for the data being erased by hot hole injection into the floating gate from the drain region or the source region. However, Hemink et al. discloses the use of electrons and hot holes for programming or erasing (column 14, lines 14-20) to increase a programming/erasing speed (column 14, lines 3-4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Lee et al. or Sakui et al. by using electrons and hot holes for programming or erasing to increase a programming/erasing speed in a non-volatile memory device.

Allowable Subject Matter

10. Claims 7, 8 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not teach the following:

wherein the erase circuit comprises high withstand pressure transistors which supply an erase potential to the bit lines, and the high withstands pressure transistors in the same block are controlled by the same column selection signal.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Noda discloses a nonvolatile semiconductor memory device having a data reprogram mode.

Ikehashi et al. discloses a nonvoltaile semiconductor memory.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Huan Hoang whose telephone number is (571) 272-1779. The examiner can normally be reached on Mon-Fri 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HH
11/17/05

Huan Hoang
Primary Examiner
Art Unit 2827